



# OPTOELECTRONICS PACKAGING FOR EFFICIENT CHIP-TO-WAVEGUIDE COUPLING

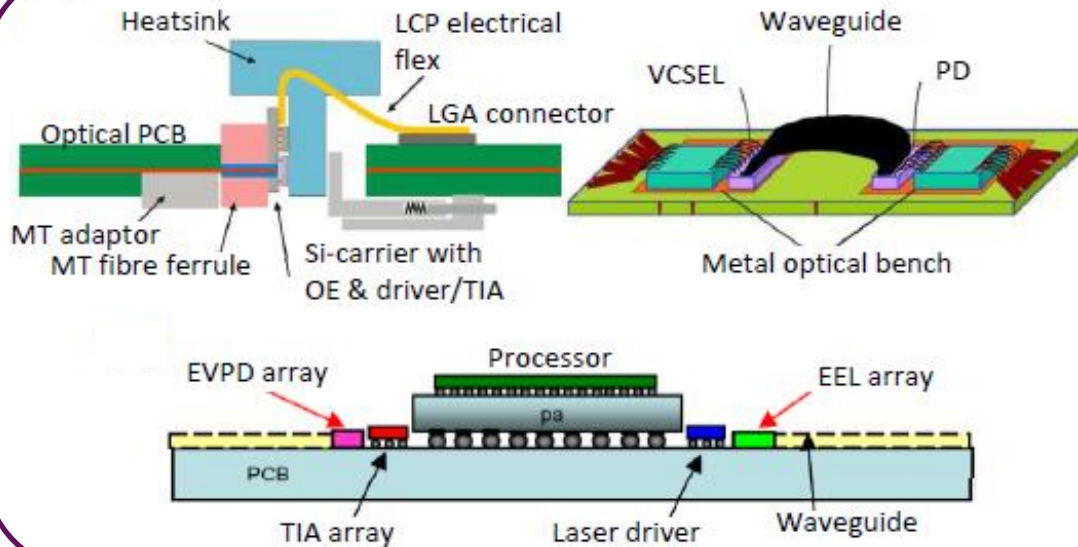
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# OPTOELECTRONICS PACKAGING

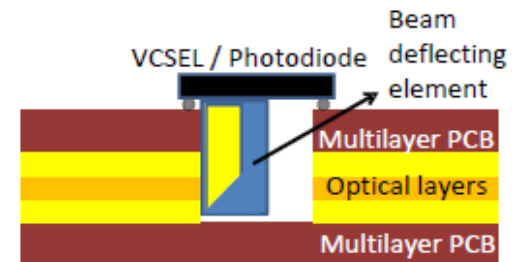
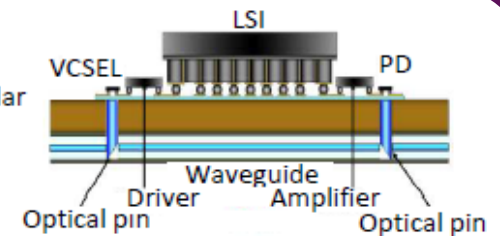
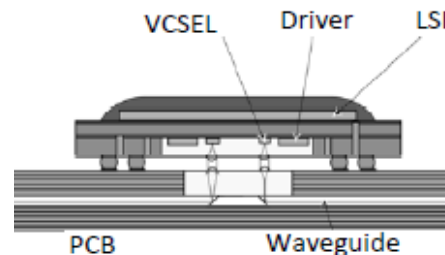
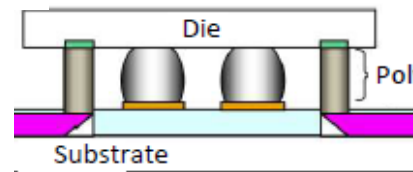


In-plane coupling approach schemes

IBM, ETRI,  
Georgia Inst. of Technol.

Vertical light confinement between optoelectronics and waveguides

Fujitsu, Tokai Univ.,  
NTT, Siemens C-LAB

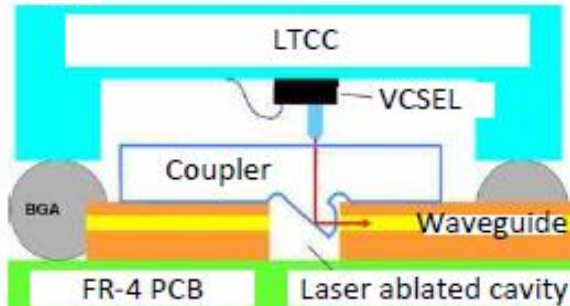
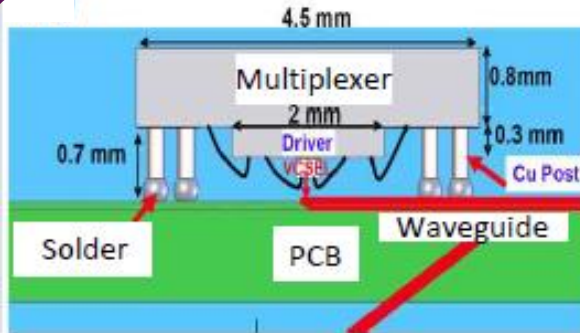


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# OPTOELECTRONICS PACKAGING

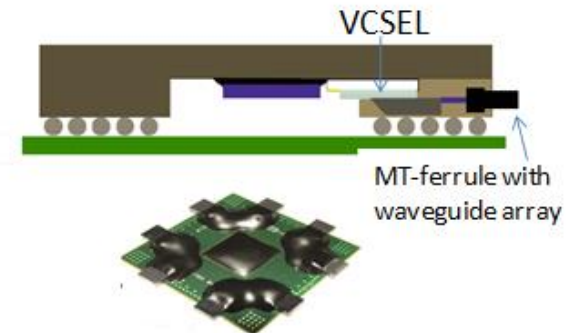
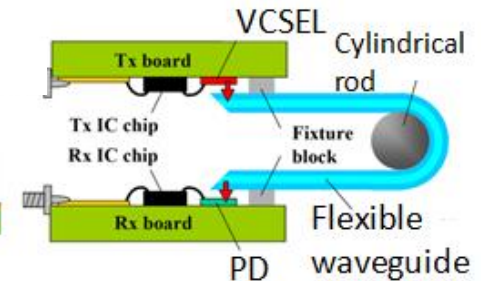
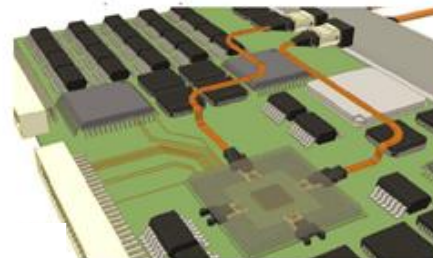
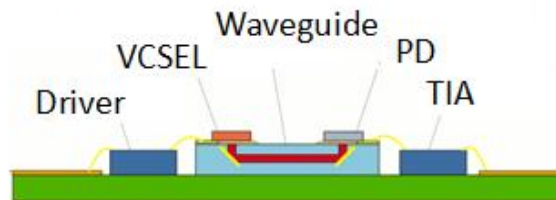


Vertical proximity coupling

*Institute of Microelectronics (Singapore), Univ. Oulu.*

Separate waveguide PCB approach

*Central Glass Co., Ltd. (Japan),  
Korea Photonics Technol. Inst.,  
Reflexphotonics*

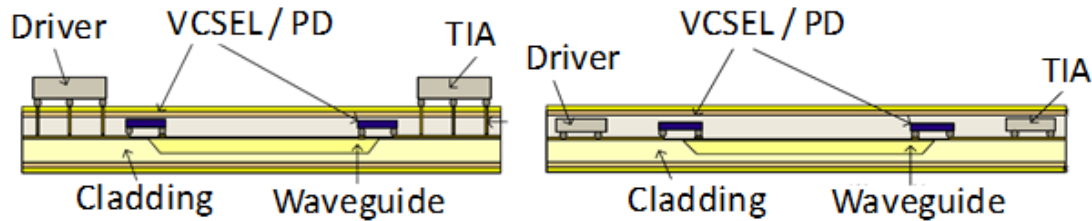


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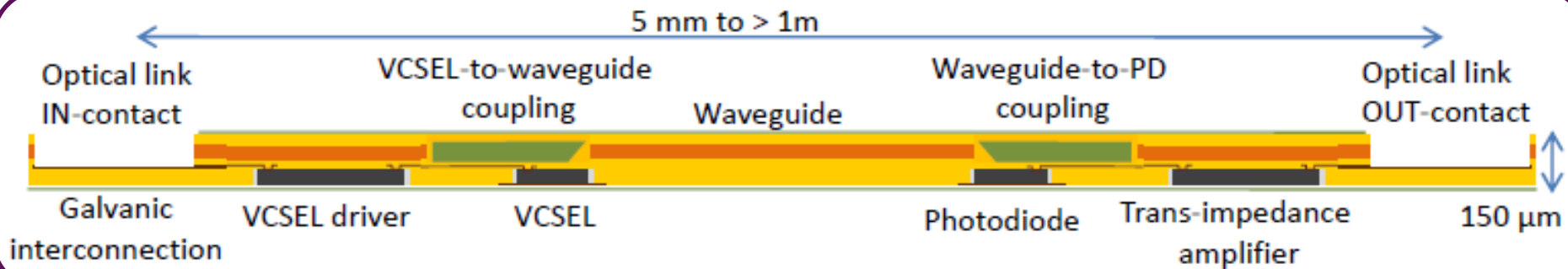
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# OPTOELECTRONICS PACKAGING



Embedding of optoelectronics in RCC laminates

*Inha Univ. (South Korea)*



Embedding of optoelectronics in flex substrates

*Ghent Univ. / imec*

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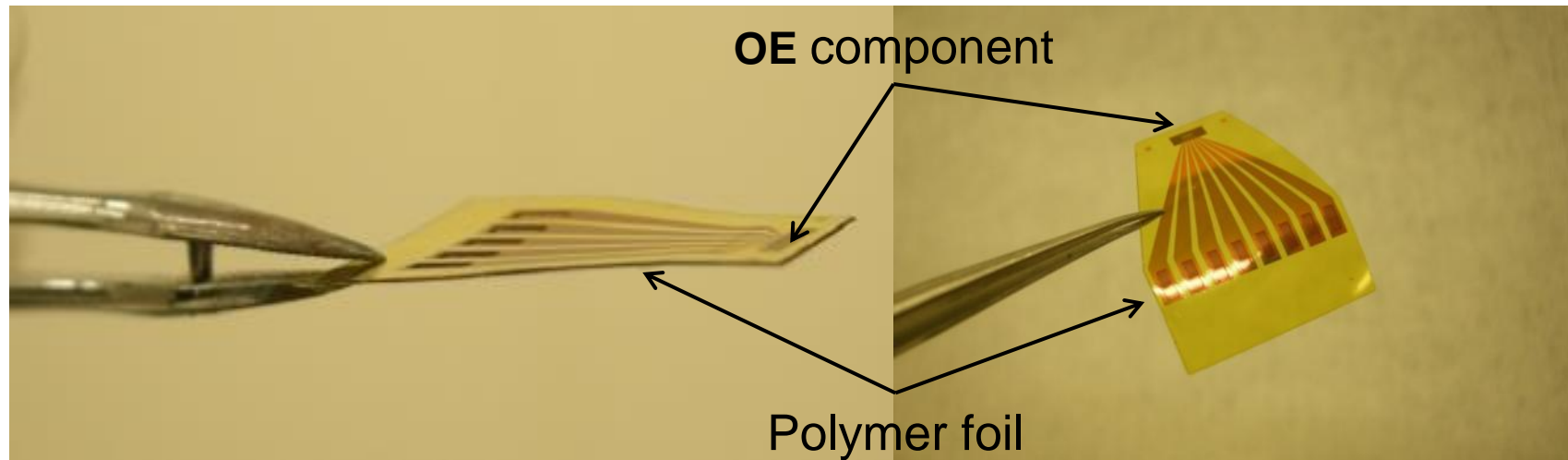
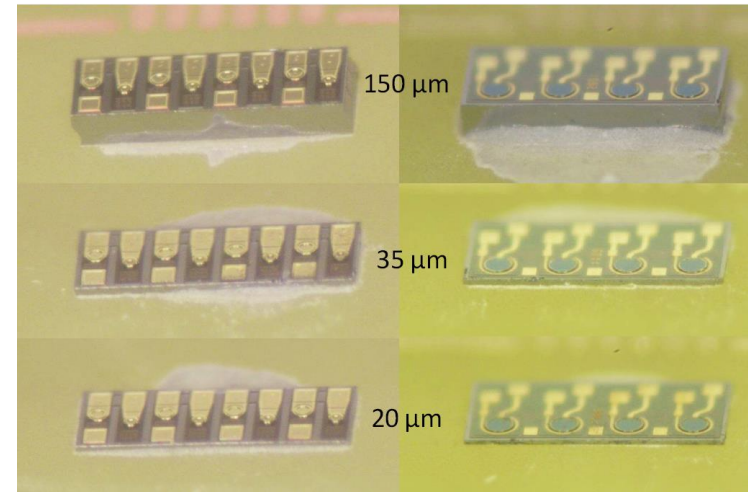
# ULTRA-THIN OPTOELECTRONIC CHIP PACKAGE

“Ultra thin optoelectronic package”

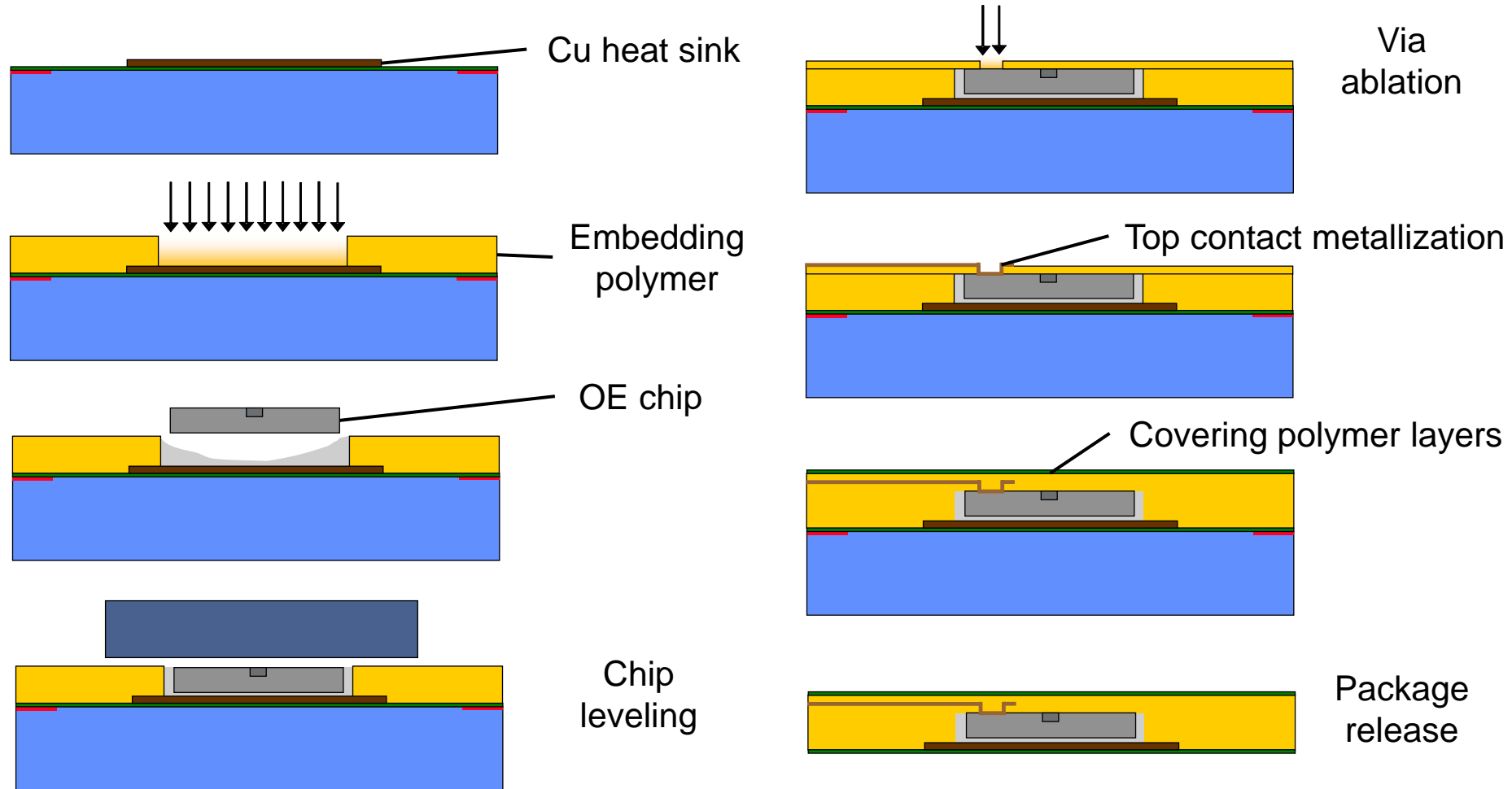
- ❖ Thinned commercial (opto)electronic components
- ❖ Embedded in **thin** & **flexible** polymer foils

Component (bare die) thickness  $\sim 20\mu\text{m}$

Total thickness  $\sim 40\mu\text{m}$



# ULTRA-THIN OPTOELECTRONIC CHIP PACKAGE



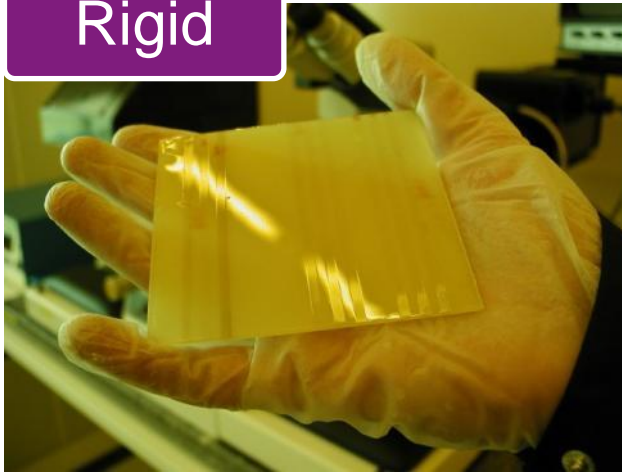
Precise process flow depends on substrate, polymer and component



# INTEGRATION WITH POLYMER OPTICAL WAVEGUIDES

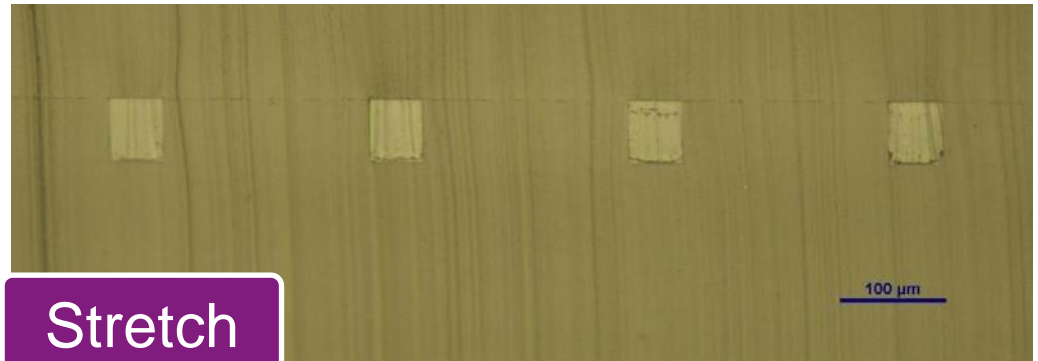
- ▶ Acrylate, epoxy, silsesquioxanes, or silicone based
- ▶ Typical propagation loss below 0.1dB/cm

Rigid

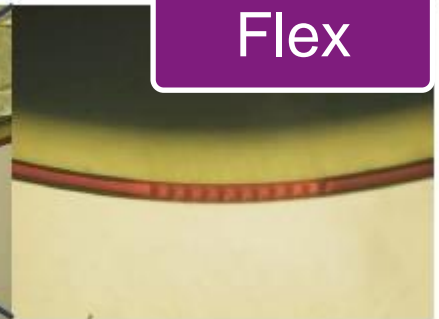
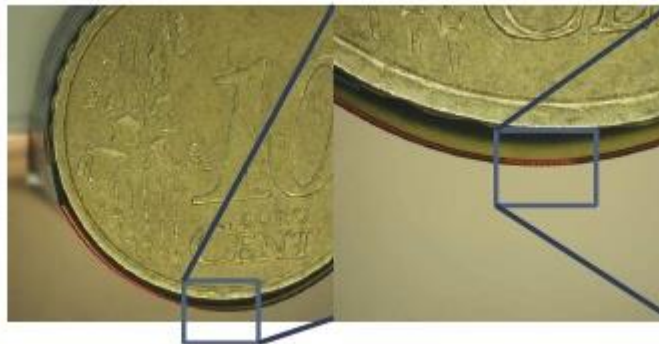
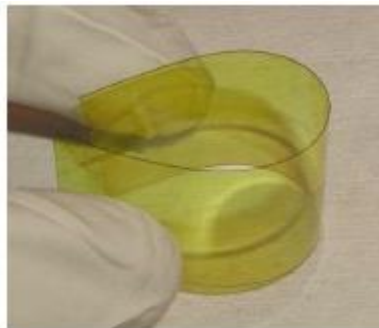


Additional bending and stretching loss

Stretch



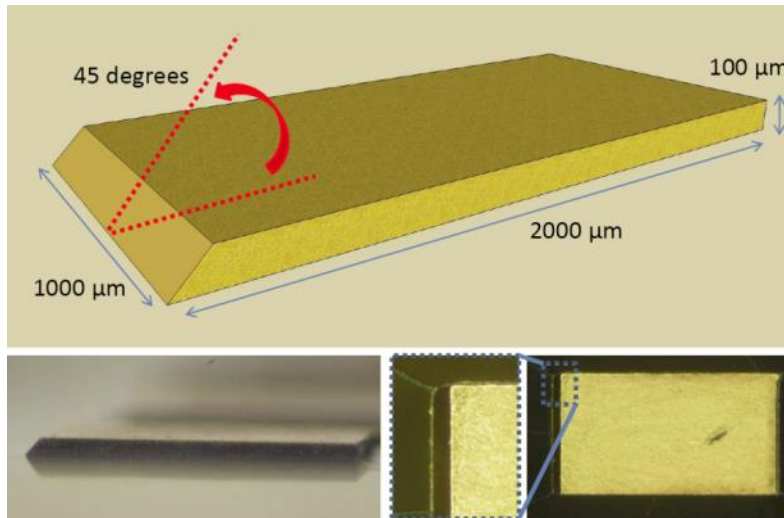
Flex



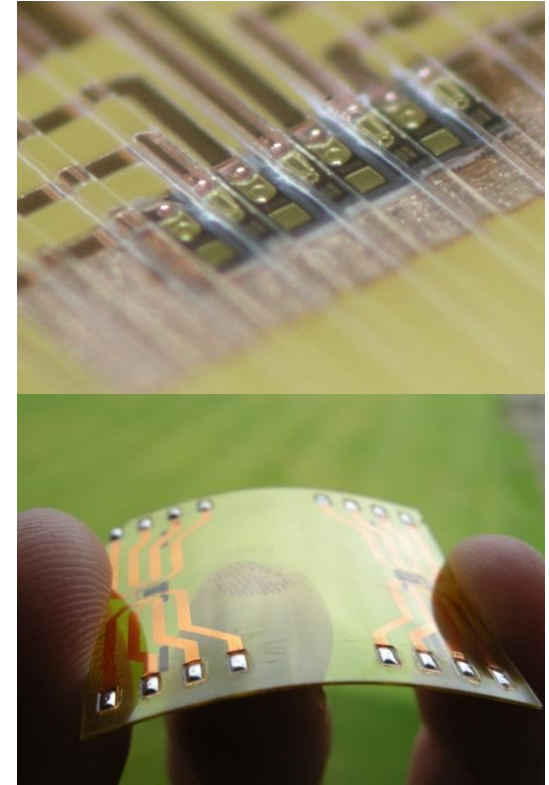
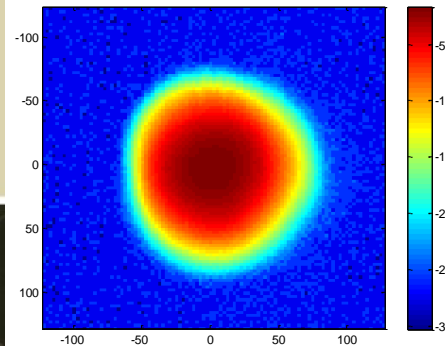
# INTEGRATION WITH POLYMER OPTICAL WAVEGUIDES

Sequential build-up approach

- ▶ Typical total optical loss 6dB



Mirror loss 0.5 dB



45 ° coupling plug

45 ° coupling plug

Signal<sub>in</sub>

Signal<sub>out</sub>



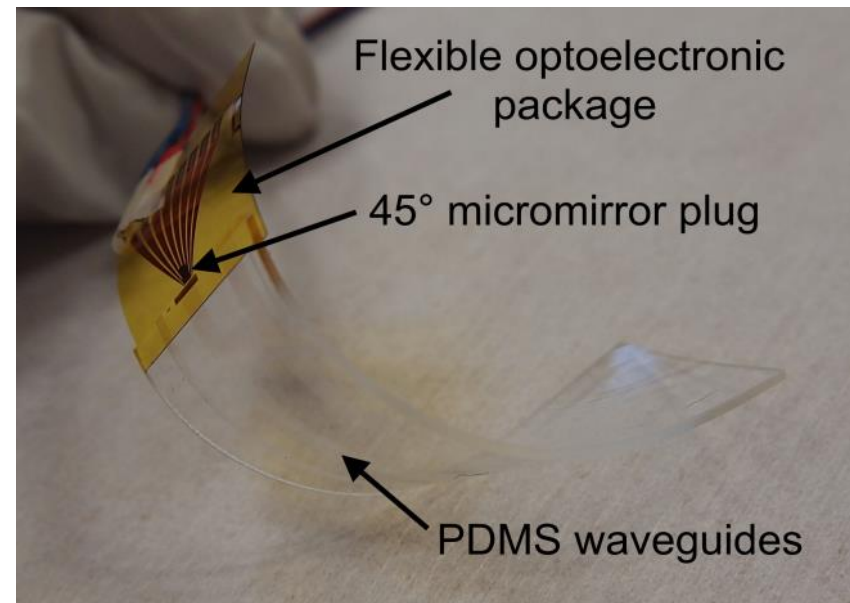
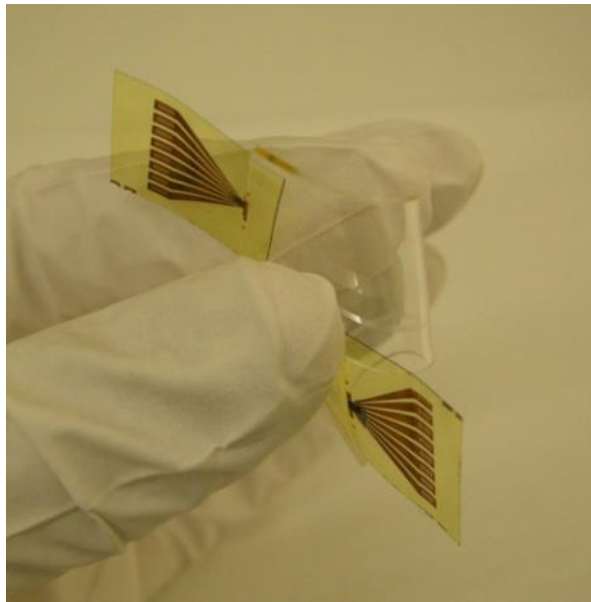


# INTEGRATION WITH POLYMER OPTICAL WAVEGUIDES

## Modular approach

- ▶ Typical total optical loss 3dB

Stretching  
up to 30%  
without  
significant  
loss

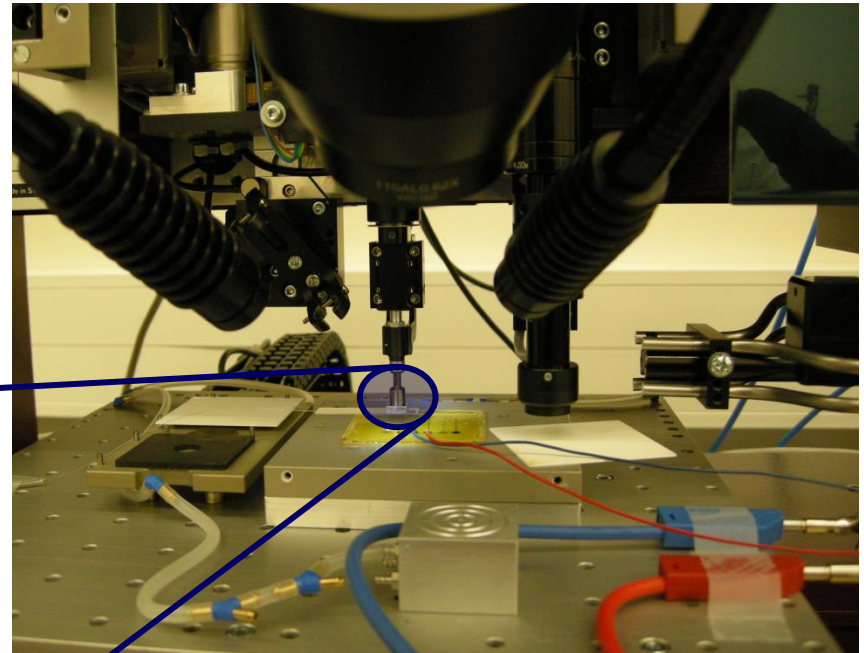
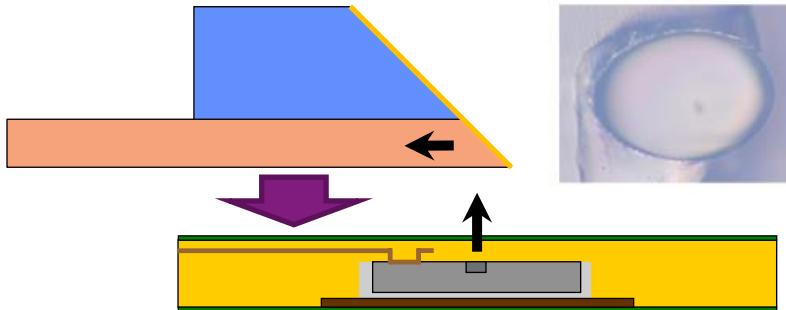


VCSEL array

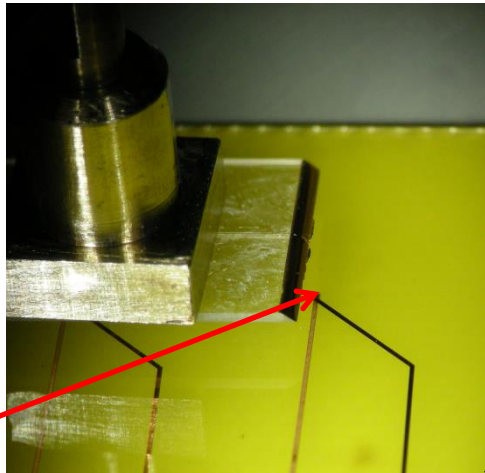
Photodiode array



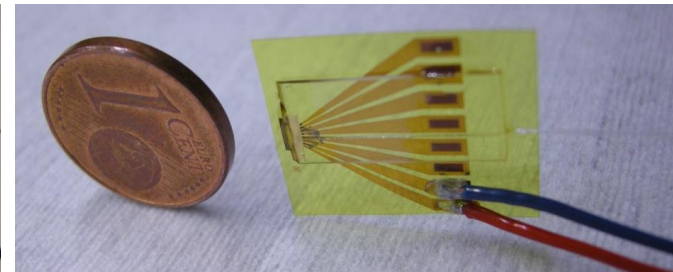
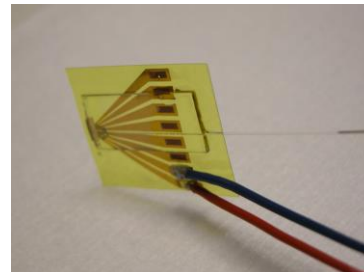
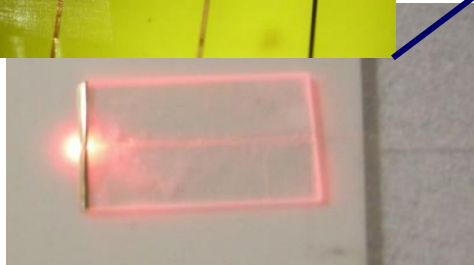
# INTEGRATION WITH OPTICAL FIBERS



assembly based on  
adapted flip chip process



OE  
component



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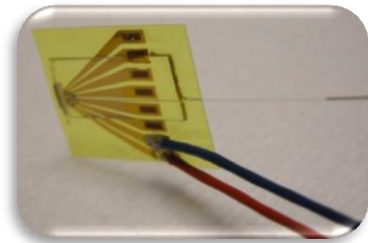
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# EU PROJECT PHOSFOS

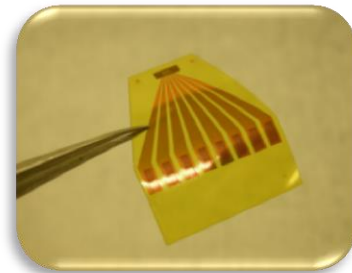
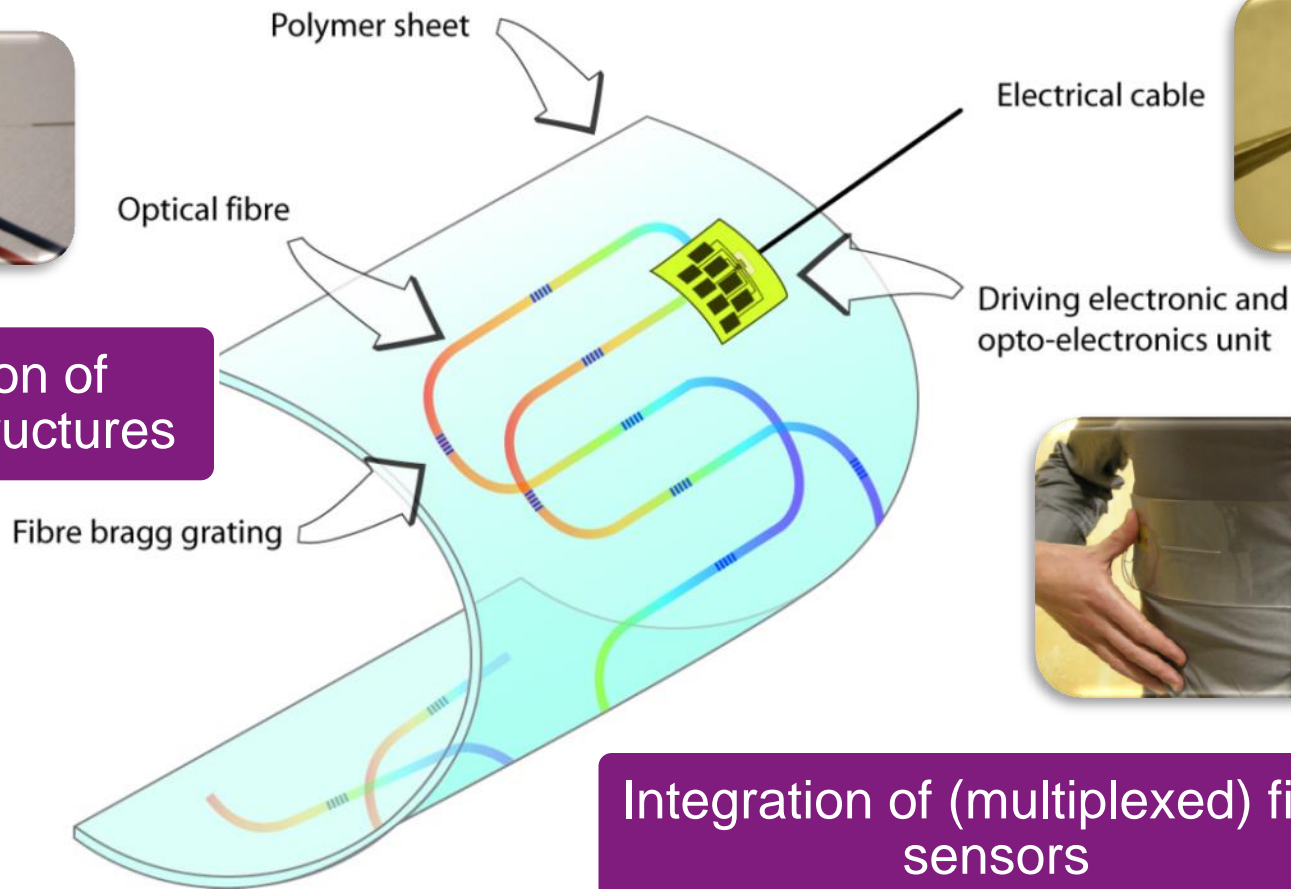
## PHOTONIC SKINS FOR OPTICAL SENSING



Integration of optoelectronic chips



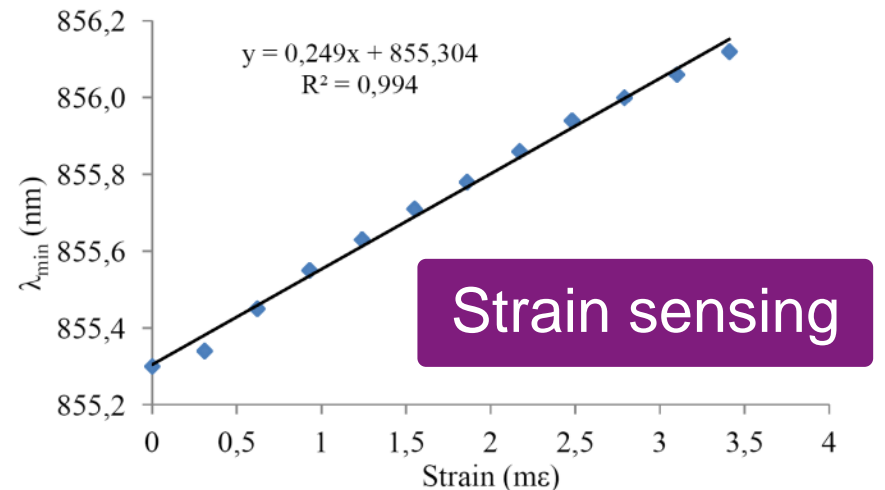
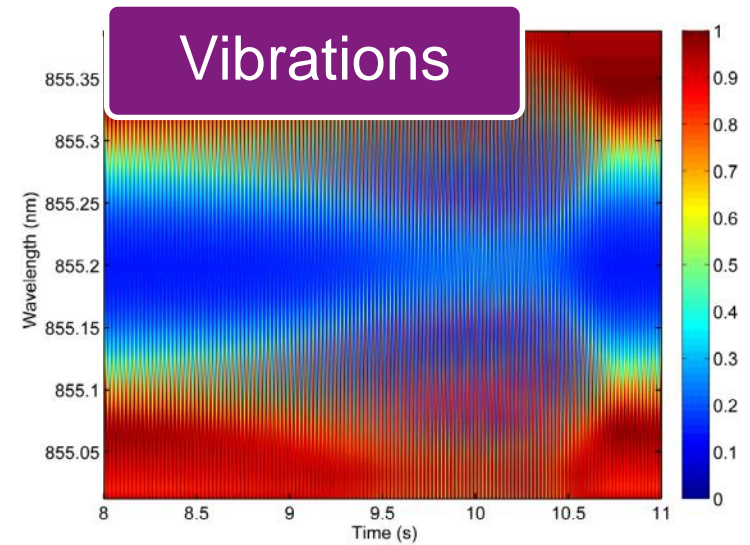
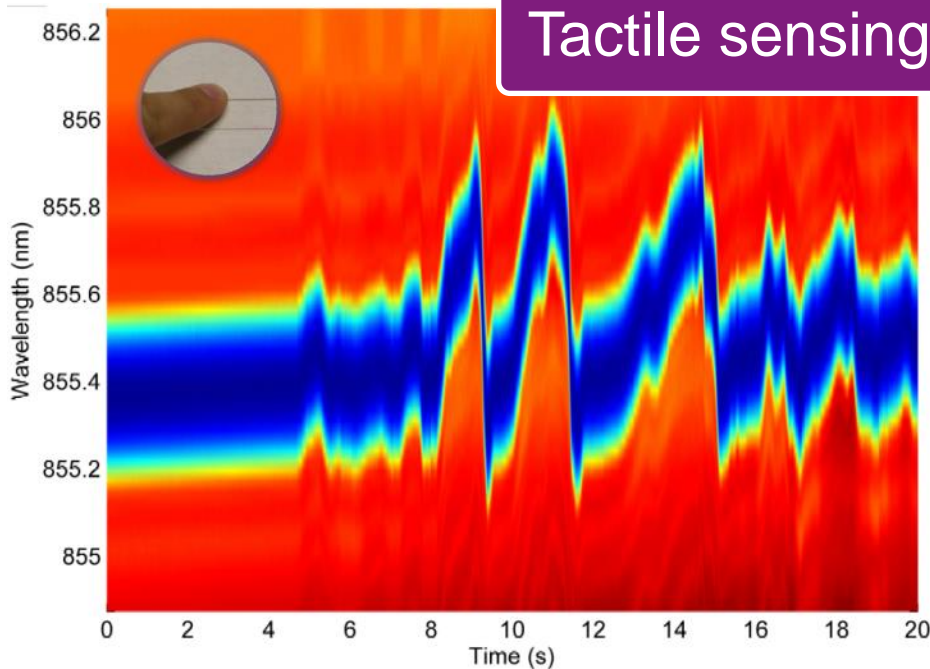
Integration of coupling structures



Integration of (multiplexed) fiber sensors

# EU PROJECT PHOSFOS

## PHOTONIC SKINS FOR OPTICAL SENSING



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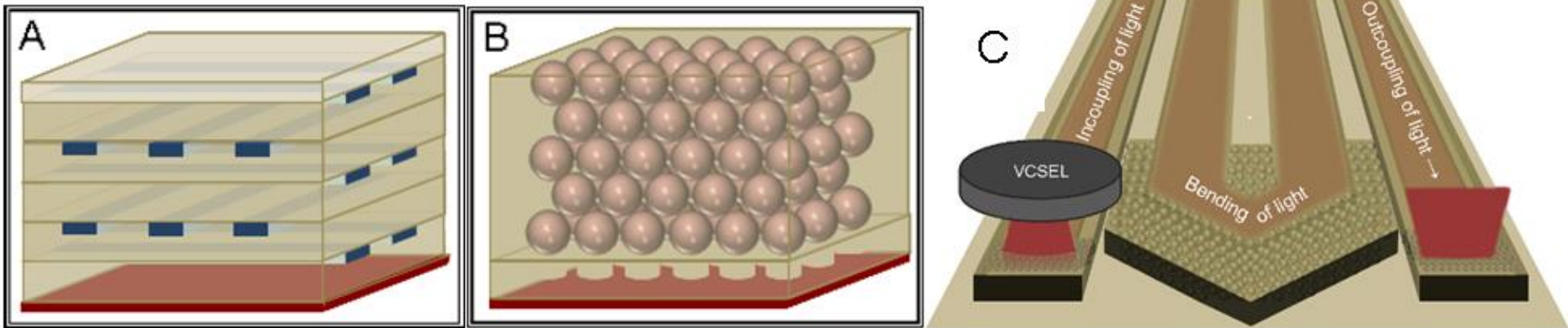
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# EU PROJECT FIREFLY MULTILAYER PHOTONIC CIRCUITS

## Challenges

- ▶ Integration of waveguides and VCSELs
- ▶ Integration of waveguides and glass fibers
- ▶ Integration of photonic crystals and waveguides



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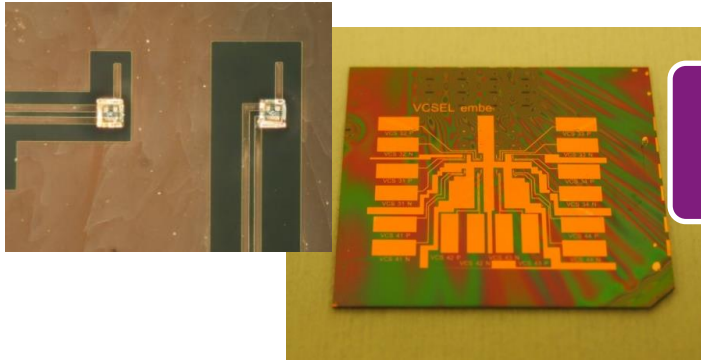


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**Multilayer Photonic Circuits made by Nano-Imprinting of Waveguides and Photonic Crystals**

# EU PROJECT FIREFLY

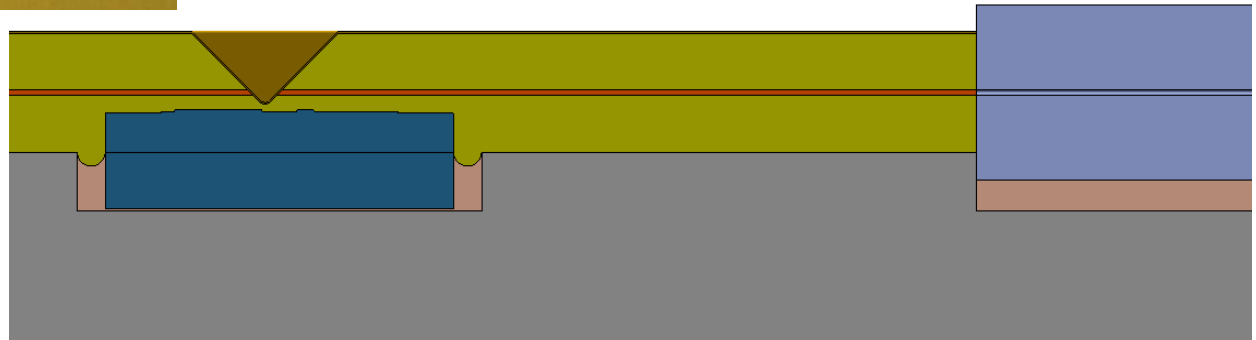
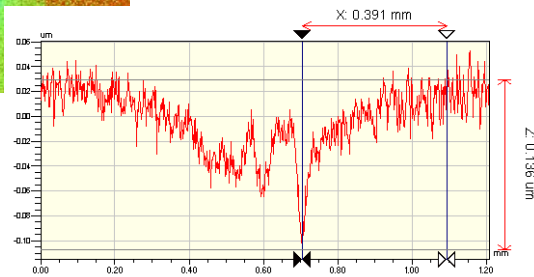
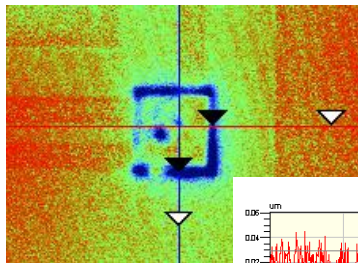
## VCSEL – WAVEGUIDE INTEGRATION



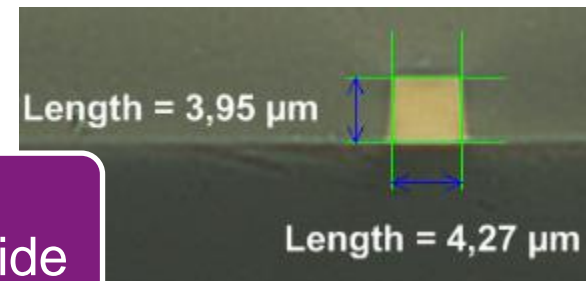
Face-up embedding  
of VCSELS



Planarity after chip  
embedding



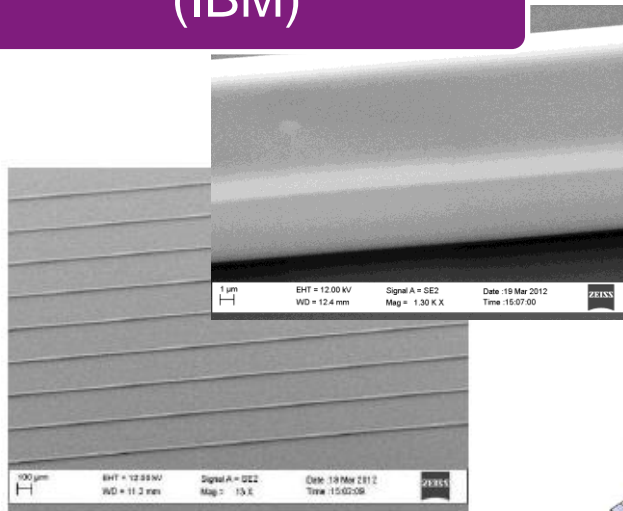
Single mode  
polymer waveguide  
technology



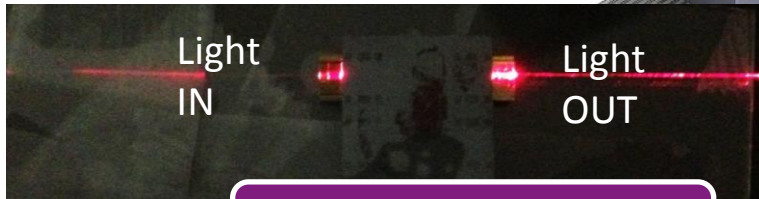
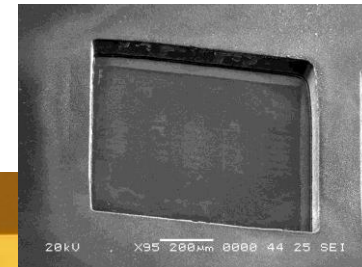
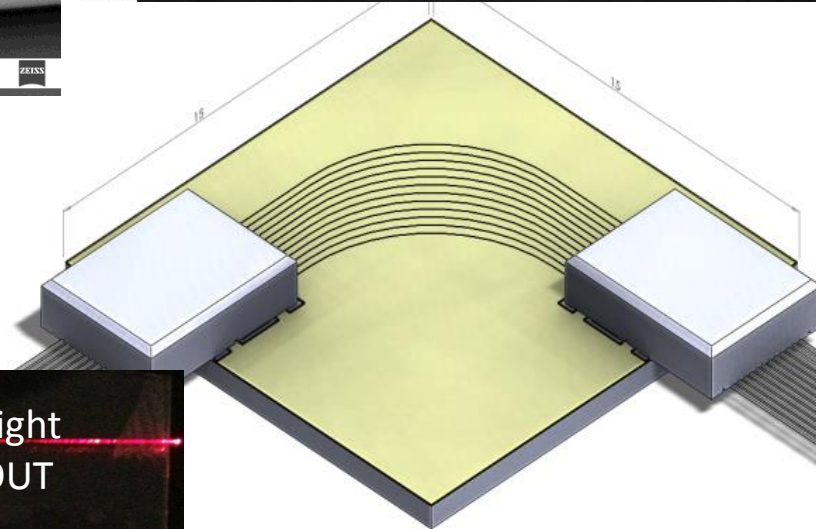


# EU PROJECT FIREFLY WAVEGUIDE – FIBER INTEGRATION

Laser direct writing  
(IBM)

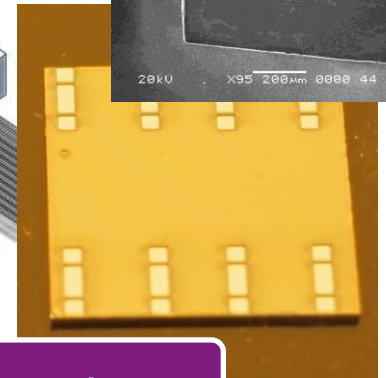


End facet  
(TE Connectivity)



Initial testing  
(TE Connectivity)

Laser cleaning



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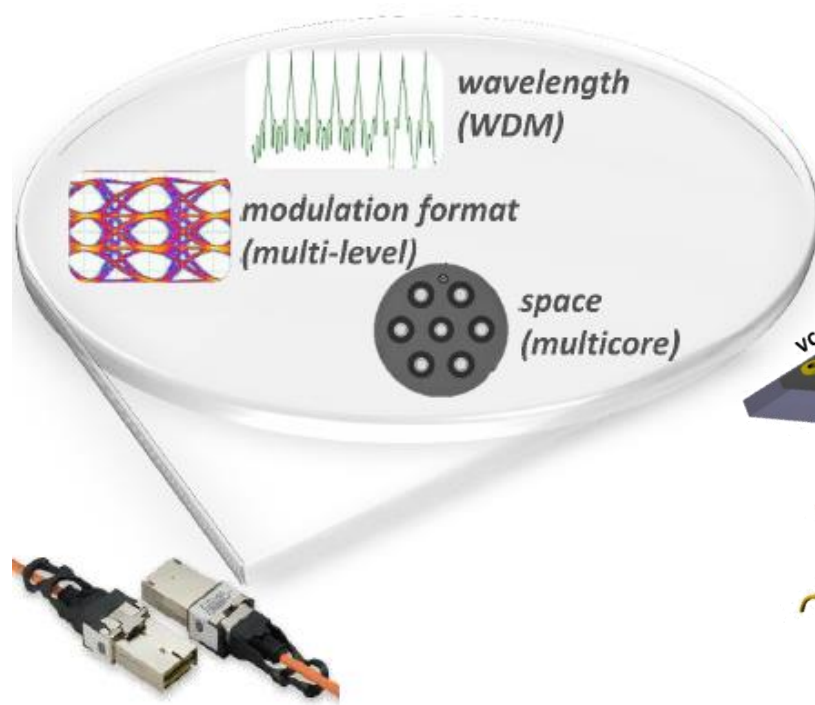
# EU PROJECT MIRAGE TERABIT CAPACITY AOC

Scale line rate to 40G

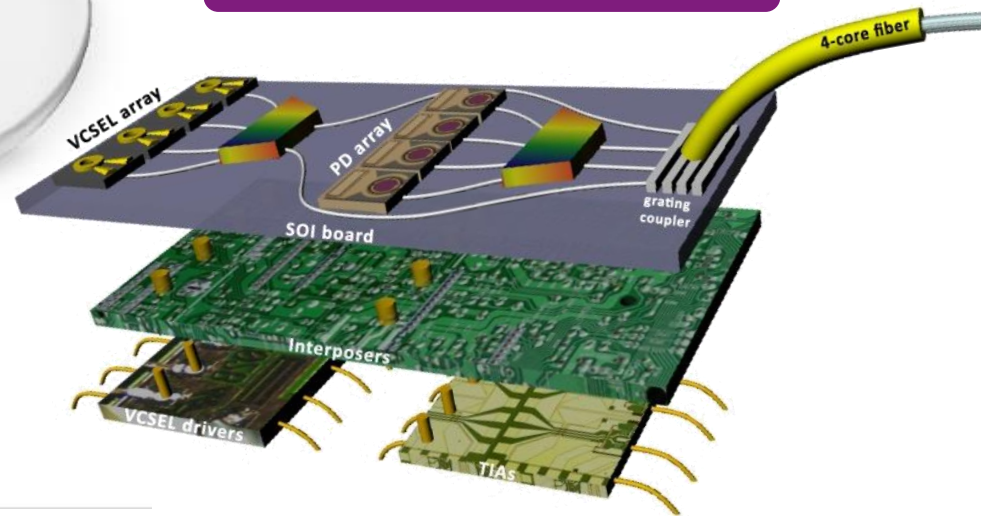


Introduce new degrees of parallelization

- WDM | multi-core | multi-level



3D photonic-electronic  
integration



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# EU PROJECT MIRAGE

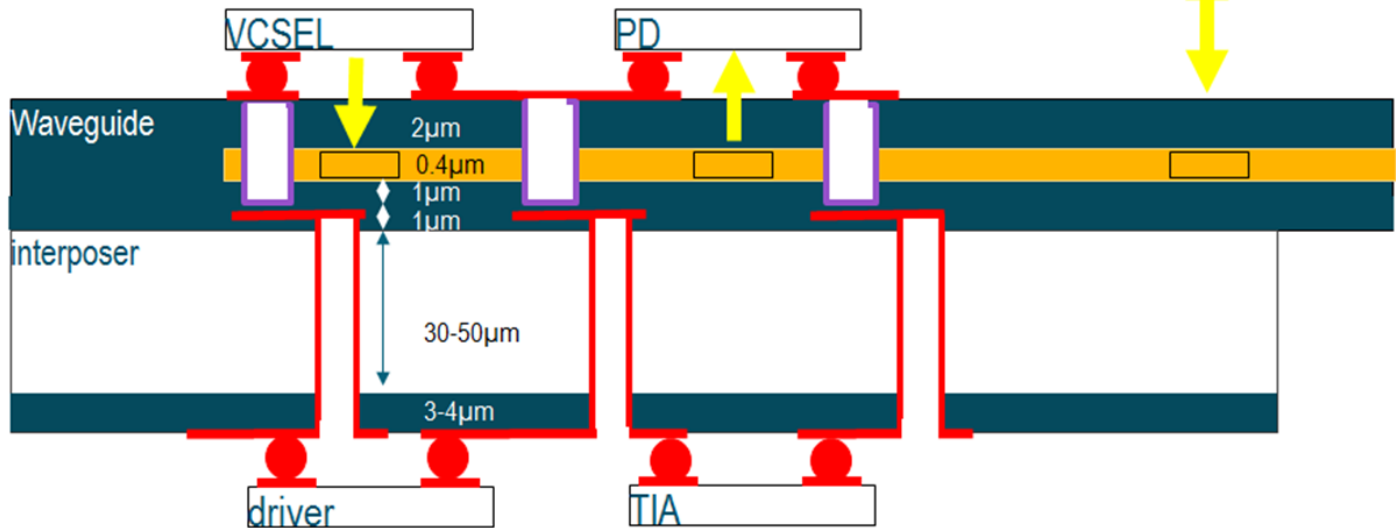
## TERABIT CAPACITY AOC

### Optoelectronics assembly

- ▶ Control of vertical separation
- ▶ Low temperature bonding
- ▶ Process flexibility (chip scale bonding, relaxed metallization requirements)



Micro-bump  
flip chip



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# EU PROJECT MIRAGE

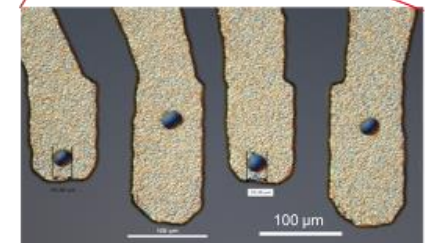
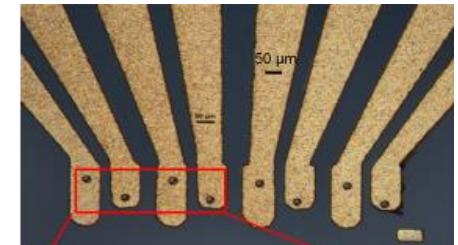
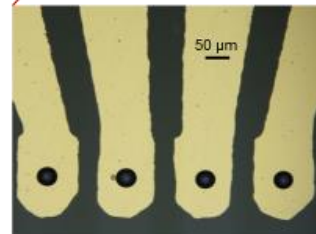
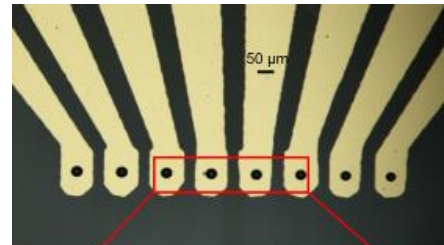
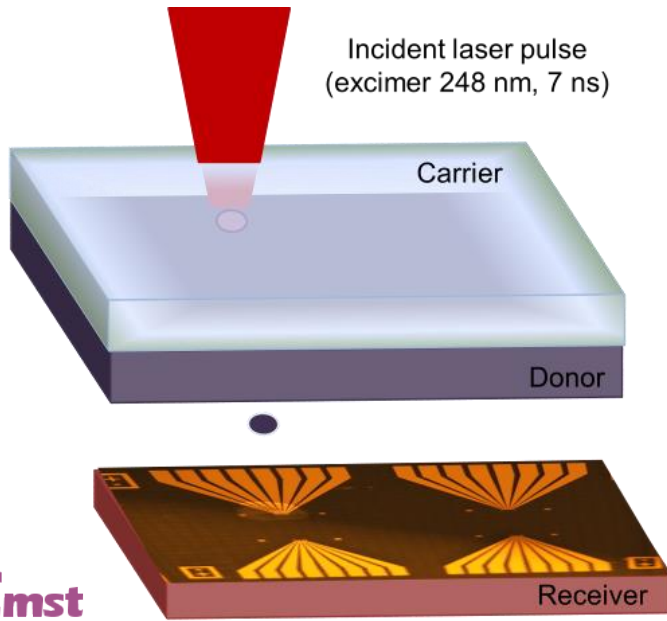
## TERABIT CAPACITY AOC

### Optoelectronics assembly



- ▶ Accurately defining micro-bumps using

#### 1 “Laser Induced Forward Transfer” (LIFT)



Adhesive bonding /  
thermocompression

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# EU PROJECT MIRAGE

## TERABIT CAPACITY AOC

### Optoelectronics assembly

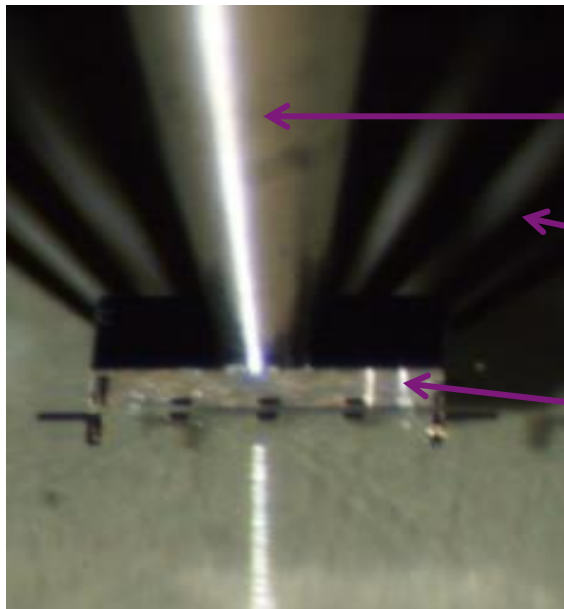


- Flip chip bonding of the die

2

= chip placement + adhesive curing

+ thermo-compression bonding

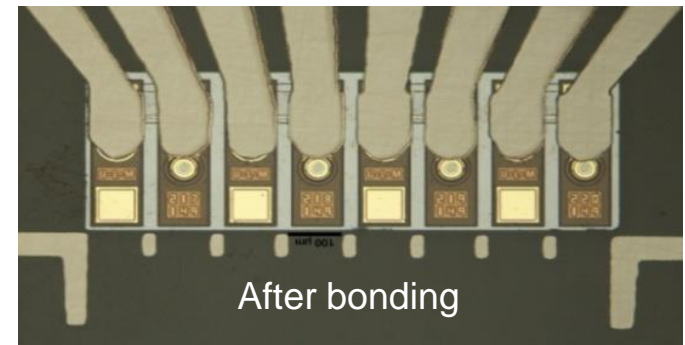


Flip chip bonder chuck

Substrate + metal  
tracks + adhesive  
bumps

OE chip (active area  
facing down)

VCSEL test chip (1x4 array)



After bonding



# EU PROJECT MIRAGE

## TERABIT CAPACITY AOC

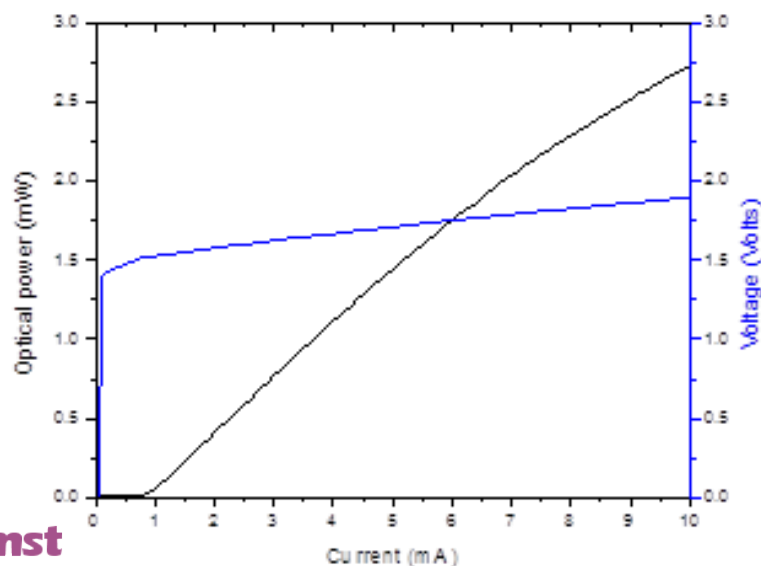
### Optoelectronics assembly



- ▶ Characterization of bonded VCSEL/PD chips
- ▶ Shear testing after bonding

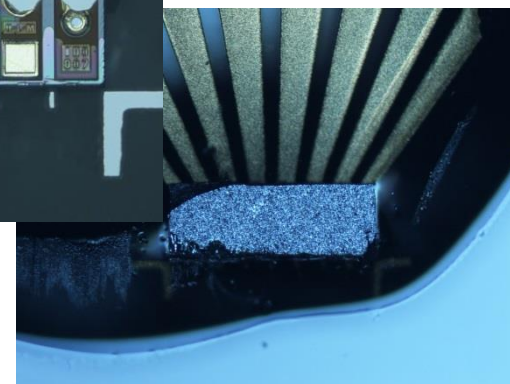
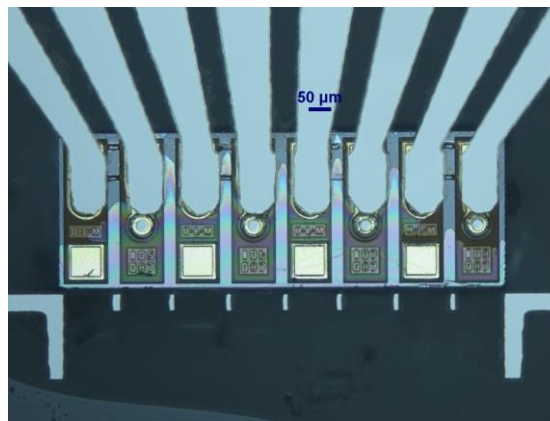
3

LVI curve for bonded test VCSELs



chip encapsulation

chip breaks during the shear test



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# ACKNOWLEDGEMENT



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**THANK YOU**

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